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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,223	02/27/2004	Fumitoshi Yamamoto	67161-142	4831

7590 10/05/2004

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,223	YAMAMOTO ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5 and 9* is/are rejected.

7)☒ Claim(s) *3,4 and 6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *27 February 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 5, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Canclini (USPN 5,341,005) in view of and further in view of Yasaitis (USPN 4,722,910) and further in view of Wolf ("Silicon Processing for the VLSI Era, Vol. 2 – Process Integration," p.12-13).

4. In reference to claim 1, Canclini (USPN 5,341,005) discloses a similar device. Figures 1 and 2 of Canclini disclose a semiconductor device with a surge protection circuit that is electrically connected to a signal input terminal (6) and has a diode (DZ) and a transistor (NPN). The device has a semiconductor substrate (2) with a main surface. Canclini does not disclose surrounding the transistors with an element isolation region such as a field oxide. However the use of element isolation regions is well known in the art. Yasaitis discloses that it

is customary for active regions to be surrounded by element isolation regions such as field oxides (column 1, lines 14-18). Furthermore Wolf ("Silicon Processing for the VLSI Era, Vol. 2 – Process Integration," p.12) discloses that isolation is critical in the implementation of silicon integrated circuits. The isolation provides devices with the advantages of lower reverse-bias junction leakages and higher breakdown voltages. In view of Yasaitis and Wolf, it would therefore be obvious to surround the device of Canclini with an element isolating region such as a field oxide on the substrate surface. A first conductive layer (12) is formed on the main surface of the semiconductor substrate (2) and is electrically connected to the signal input terminal (6). The diode has a cathode which includes a first cathode region (5) and a second cathode region (3 or 6). The first cathode region (5) is formed at the main surface of the substrate (2). The first cathode region (5) and the second cathode region (3 or 6) together with an anode region (7) of the diode form a pn junction where Zener breakdown occurs.

5. With regard to claim 2, the cathode (5) and a collector (5) of the transistor are electrically connected to the signal input terminal (6). The anode (7) and the base (7) are formed to be of the same conductivity type and are electrically connected to each other.

6. In reference to claim 5, the anode region (7) and the second cathode region (3 or 6) which constitute the pn junction where Zener breakdown occurs are both formed in an epitaxial layer (1) formed in the substrate (column 2, lines 49-52).

7. With regard to claim 9, the transistor has a collector including an epitaxial layer (1) and a diffusion layer (5) formed within it. The diffusion layer (5) has a higher impurity concentration than the epitaxial layer (1).

Allowable Subject Matter

8. Claims 3, 4, and 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a semiconductor device having a surge protection circuit with a Zener diode and a bipolar transistor such that the Zener diode has a cathode region connected to a terminal and additional cathode regions in a semiconductor substrate which surround an anode region in the semiconductor substrate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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